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73M1866B/73M1966B PCM Connectivity

Introduction

Some PCM equipment reference their timing on the PCM clock (PCLK) rising edge that precedes the first falling edge of PCLK that follows the assertion of frame sync (FS). This document refers to this timing method as the *frame-sync reference method*. The 73M1866 and 73M1966 use the first falling PCLK edge after the assertion of FS to reference their timing. This application note describes how to configure and use the 73M1x66 with equipment that uses the frame-sync reference method.

The 73M1866B/73M1966B PCM highway benefits from the following features, which ensure connectivity with all PCM interfaces:

- Linear and compressed modes.
- Master and slave modes.
- Transmit time and clock slots.
- Receive time and clock slots.
- Transmit and receive edge selection.
- Half bit drive for bit 0.
- PCLK frequency selection.
- PCM transmit enable.

FS reference timing equipment and the 73M1866B/73M1966B have different numbering schemes to designate the time at which PCM data is transmitted to or received from the PCM highway.

The key parameters to align between FS reference timing equipment and the 73M1866B73M1966B are the time and clock slots and the clock edge polarity for receive and transmit paths. Within a PCM frame, the transmission (reception) of an 8- or 16-bit data sample can start at any bit slot during that frame and with respect to either the rising or falling edges of PCLK. The 73M1866B/73M1966B bit numbering is slightly off from that of FS reference timing equipment, thus requiring mapping between the two numbering schemes.

Other parameters, such as linear and compressed modes, LSB half-bit drive, master and slave modes, and PCM enable do not need any translation between timing reference modes.

Mapping

Figure 1 represents the 73M1866B/73M1966B bit numbering around the FS pulse.

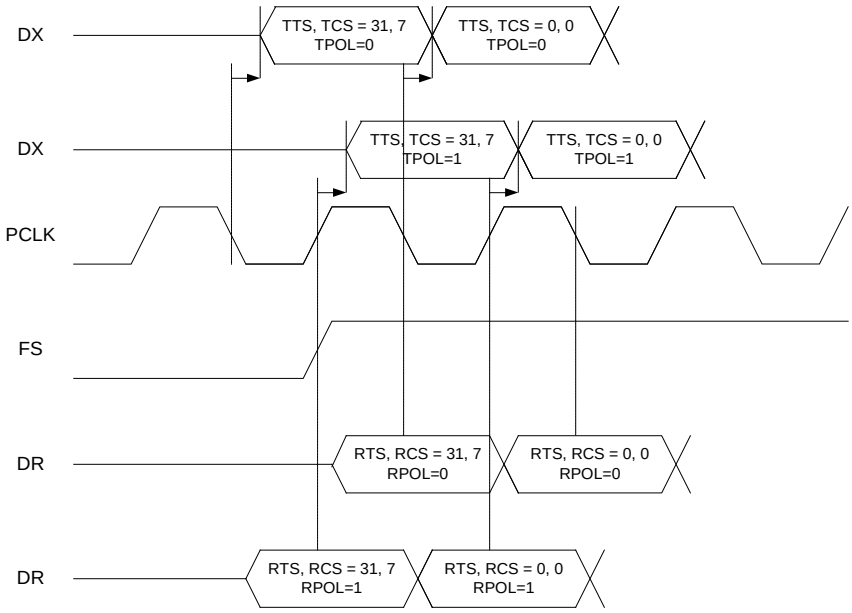

Figure 1: 73M1866B/73M1966B PCM Frame Bit Numbering

The 73M1866B/73M1966B PCM settings must be complementary to those of PCM. In other words, FS reference timing transmitter settings define what the 73M1866B/73M1966B receiver PCM settings must be. The same applies to FS reference timing receiver settings and the 73M1866B/73M1966B transmitter settings. The conversion is illustrated in Table 1 and Table 2.

Table 1: Transmitter to 73M1866B/73M1966B Receiver Settings for PCLK Frequency of 2.048MHz

PCM	73M1866B/73M1966B		
Transmit Time Slot	Receive Time Slot	Receive Clock Slot	Receive Edge Polarity
	RTS[5:0]	RCS[2:0]	RPOL
0	31	7	0
1	0	7	0
2	1	7	0
3	2	7	0
4	3	7	0
5	4	7	0
6	5	7	0
7	6	7	0
8	7	7	0
9	8	7	0
10	9	7	0
11	10	7	0
12	11	7	0
13	12	7	0
14	13	7	0
15	14	7	0
16	15	7	0
17	16	7	0
18	17	7	0
19	18	7	0
20	19	7	0
21	20	7	0
22	21	7	0
23	22	7	0
24	23	7	0
25	24	7	0
26	25	7	0
27	26	7	0
28	27	7	0
29	28	7	0
30	29	7	0
31	30	7	0

Table 2: Receiver to 73M1866B/73M1966B Transmitter Settings for PCLK Frequency of 2.048MHz

PCM	73M1866B/73M1966		
Receive Time Slot	Transmit Time Slot	Transmit Clock Slot	Transmit Edge Polarity
	TTS[5:0]	TCS[2:0]	TPOL
0	31	7	1
1	0	7	1
2	1	7	1
3	2	7	1
4	3	7	1
5	4	7	1
6	5	7	1
7	6	7	1
8	7	7	1
9	8	7	1
10	9	7	1
11	10	7	1
12	11	7	1
13	12	7	1
14	13	7	1
15	14	7	1
16	15	7	1
17	16	7	1
18	17	7	1
19	18	7	1
20	19	7	1
21	20	7	1
22	21	7	1
23	22	7	1
24	23	7	1
25	24	7	1
26	25	7	1
27	26	7	1
28	27	7	1
29	28	7	1
30	29	7	1
31	30	7	1

Revision History

Revision	Date	Description
1.0	1/31/2008	First publication.